Logic Probe

Parameter \ Model	SPL2016	SLA1016
		
Input Channels	16	16
Input Impedance	100 kΩ‖18 pF	100 kΩ‖8 pF
Maximum Input Voltage	±50 V Peak	±20 V Peak
Input Dynamic Range	±20 V	±10 V
User defined threshold range	-10 V~10 V (10 mV steps)	-8 V~8 V (10 mV steps)
Threshold Selections	TTL (1.5 V) CMOS (2.5 V) 3.3 V_LVCMOS (1.65 V) 2.5 V_LVCMOS (1.25 V)	TTL (1.5 V) CMOS (2.5 V) 3.3 V_LVCMOS (1.65 V) 2.5 V_LVCMOS (1.25 V)
Threshold Accuracy	± (3% of threshold setting +200 mV)	± (3% of threshold setting +150mV)
Threshold Groupings	Group 2: D15-D8	Group 2: D15-D8
	Group 1: D7-D0	Group 1: D7-D0
Minimum Input Voltage Swing	800 mVpp	800 mVpp
Maximum Input Data Rate	300 Mbps	120 Mbps
Minimum Detectable Pulse Width	3.3 ns	8.3 ns
Channel-to-Channel Skew	±1 digital sample interval	±1 digital sample interval